BROADBAND 0.25 MICRON ION-IMPLANT MMIC LOW NOISE AMPLIFIERs ON GaAs

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ABSTRACT

A highly manufacturable 0.25 micron ion-implant-process has been used for the development of low noise MMIC amplifiers covering the 2-18 GHz band. Noise figures of less than 2.5 dB and 3.0 dB have been achieved with MMICs covering the 2-6 GHz and 6-18 GHz bands respectively. Insertion gains were 16 dB for the 2-6 GHz design and 10 dB for the 6-18 GHz design. This performance is comparable to that reported for HEMT processes.

INTRODUCTION

The purpose of this paper is to report on a family of low noise ion-implant-process amplifiers with less than 3 dB noise figure over the 6-18 GHz band and less than 2.5 dB noise figure over the 2-6 GHz bandwidth. This is believed to be the lowest noise figure performance reported over these bandwidths, using an ion-implant-process on GaAs. The measured performance is comparable to that reported for HEMT structures [1]. A unique feature of the work is the development of a highly manufacturable process using a bi-level, e-beam written, enhanced cross section gate process. The result is state of the art performance that can readily be manufactured for wide applications.

Broadband low noise amplifiers find many applications, including receive modules of electronic warfare systems. In addition to low noise figure, high gain is desired to minimize the second stage contribution on the overall receiver noise figure. MMIC amplifiers provide a substantial size-reduction and lower-cost when used in place of MIC (hybrid) designs. Use of an ion-implant-process, on GaAs, provides a low risk approach. The balanced 6-18 GHz amplifier reported in this paper is used in a wideband Transmit/Receive module.

The development of these amplifiers is described, including the fabrication process and the circuit design concepts. Presented is a 2-6 Ghz single-ended amplifier, a 6-18 GHz single-ended, and a 6-18 GHz balanced amplifier. Modelling techniques and circuit performance are also reported.

PROCESS DEVELOPMENT

These amplifiers are manufactured using electron beam lithography to define the gate electrode, all other layers are defined using established optical lithography processes developed at Lockheed Sanders for MMIC manufacture. The gate electrode is fabricated using a bi-layer resist scheme and direct write electron beam lithography(e-beam). The process consists of a 0.25 micron "T" cross-section gate, with a 0.75 micron mushroom head (figure 1).

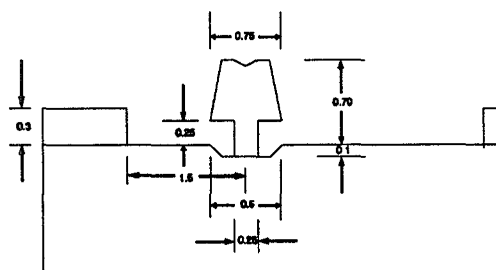

Figure 1. Gate Layout

Standard MMIC process features include bulk resistors, passivation, air bridges, 5 mil thinned substrates, and via hole grounding. A conventional ion-implanted process with a single energy Silicon 28 implant at 100Kev yielding a sheet resistance of 400 Ohm/square was used. A buried P layer Be co-implant is used to sharpen the tail. Resistors are formed from the same 400 Ohm/square N active layer used for FETs, giving excellent uniformity and reproducibility.

2-6 GHz SINGLE-ENDED DESIGN

This amplifier is a 2-6 GHz, 2-stage, reactive match design with a dual/parallel bias configuration, biased at 25% IDSS. The schematic and chip photograph for this amplifier are illustrated in figures 2 and 3. The biasing scheme allows the quiescent bias point to be set for optimum amplifier noise performance. The primary focus of circuit design is placed on

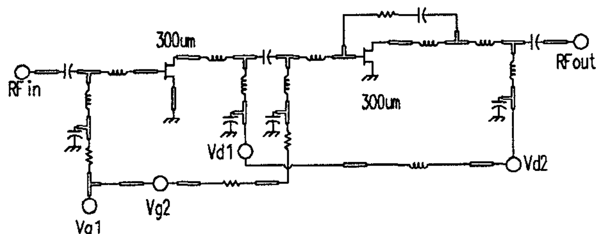

Figure 2. 2-6 GHz Single-Ended LNA Schematic

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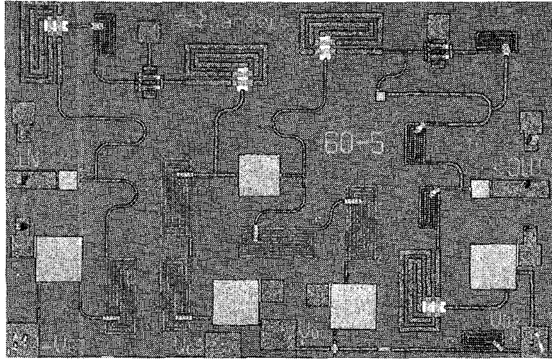

Figure 3. 2-6 GHz Single-Ended LNA Chip

achieving the lowest noise figure possible, allowing the match to degrade with the intention of use in a balanced topology.

The input matching circuit is designed to provide the optimum impedance, for minimum noise figure, of the first stage FET. Source inductance, in the form of a transmission line, is used to provide stability with no degradation in noise figure. Due to the broad bandwidth, simultaneous matching for both noise and gain using source inductance [2], is not attempted.

The interstage matching circuit is designed for three purposes. It conjugately matches the output of the first stage FET for maximum gain while simultaneously providing a good noise match for the input of the second stage FET. Some FET gain slope compensation is also provided in this circuit.

The output matching circuit is designed simultaneously for additional FET gain slope compensation and conjugate matching of the second stage FET output. Final FET gain slope compensation is achieved by the use of parallel feedback on the second stage FET. This feedback has a minimal impact on noise figure, and combined with the series source inductive feedback on the first stage provides unconditional stability for the amplifier.

The performance across a wafer, for insertion gain and noise figure, is shown in figures 4 and 5. Due to the variation

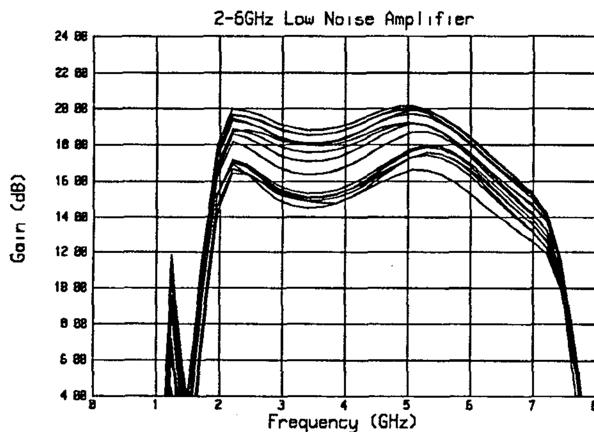

Figure 4. Single-Ended LNA Insertion Gain

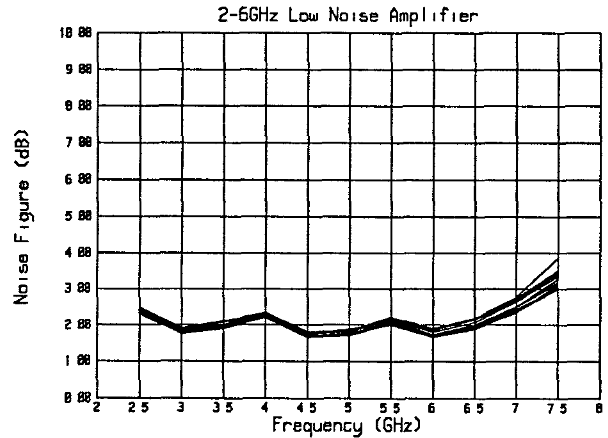

Figure 5. Single-Ended LNA Noise Figure

of Gm for the fixed gate voltage of 0.5 being higher than expected, the gain variation from site to site is 4.5 dB. The noise figure variation from site to site is less than 0.25 dB with a maximum noise figure of 2.5 dB over the 2-6 GHz band.

6-18 GHz SINGLE-ENDED AMPLIFIER

This amplifier is a 6-18 GHz, 2-stage, reactive match design utilizing source inductive feedback in the first stage and parallel feedback in the second stage. The schematic and chip photograph for this amplifier are illustrated in figures 6 and 7. The design goal for this amplifier is to minimize the overall noise figure and to maintain a minimum gain of 10 dB

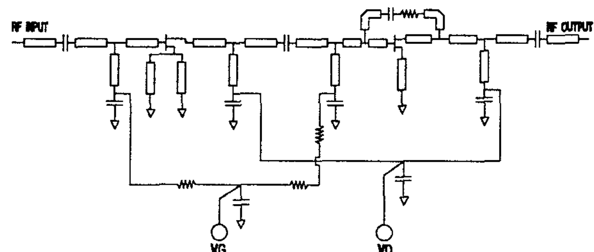

Figure 6. 6-18 GHz Single-Ended LNA Schematic

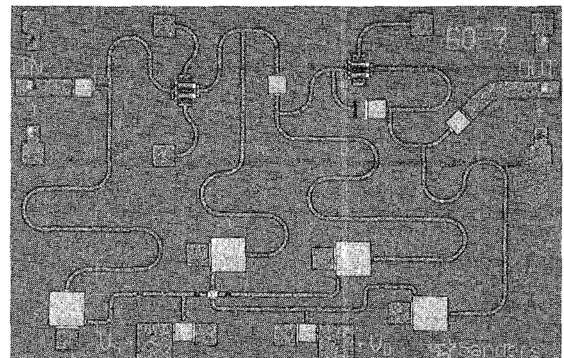

Figure 7. 6-18 GHz Single-Ended LNA Chip

with +/-1dB gain variation over frequency. The FET bias point was selected to be 50%Idss in order to improve the overall noise measure of the amplifier. This bias point also improves the 1 dB compressed power performance of the amplifier, increasing its spurious free dynamic range.

The source inductive feedback was used to improve the match (and therefore gain) at the high end of the frequency range while still providing the optimum noise match at these frequencies. The amount of resistive feedback used in the second stage was minimal and was used for stability and gain shaping.

The performance across a wafer, for insertion gain and noise figure, is shown in figures 8 and 9. The gain variation from site to site is 2.0 dB. The noise figure variation from site to site is less than 0.25 dB with a maximum noise figure of 3 dB over the 6-18 GHz band. The predicted data, using measured FET parameters of devices from the fabricated wafer, closely tracks the measured data.

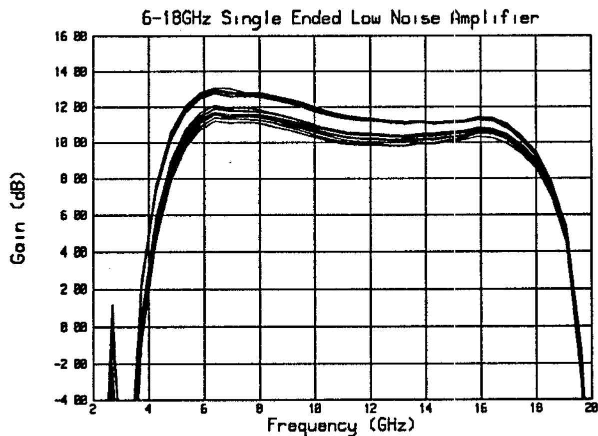

Figure 8. Single-Ended LNA Insertion Gain

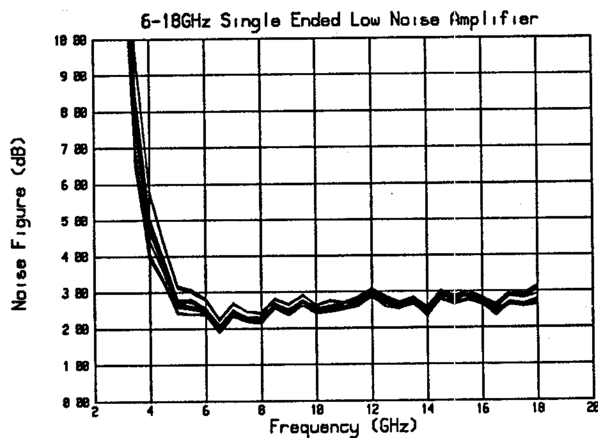

Figure 9. Single-Ended LNA Noise Figure

BALANCED AMPLIFIER

To provide an LNA with a good VSWR, the 6-18 GHz single-ended design was balanced with an optimized on-chip coupler. The lengths of many transmission lines were adjusted to optimize the performance of the coupler. The coupler topology is a wilkinson divider with an additional capacitor and the output arms are low and high pass circuits to give a 90 degree difference for isolation. The loss through the coupler is just 0.5 dB. The schematic and chip photograph for this amplifier are illustrated in figures 10 and 11.

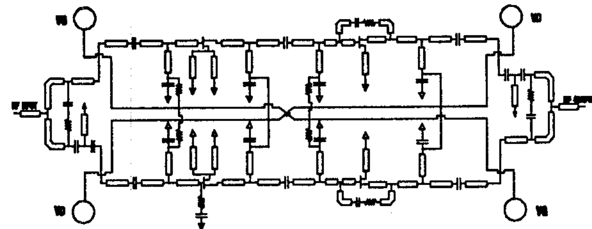

Figure 10. 6-18 GHz Balanced LNA Schematic

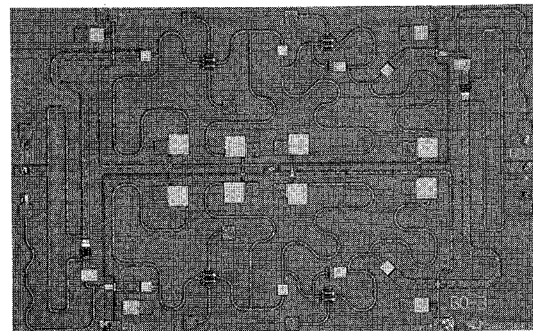

Figure 11. 6-18 GHz Balanced LNA Chip

The performance across a wafer, for insertion gain and noise figure, is shown in figures 12 and 13. The gain variation from site to site is 2.0 dB. The noise figure variation from site to site is less than 0.5 dB with a maximum noise figure of 3.5

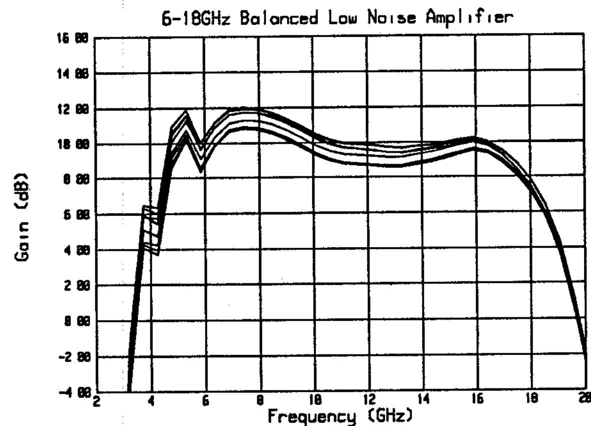

Figure 12. Balanced LNA Insertion Gain

dB over the 6-18 GHz band. The input and output reflection is shown in figures 14 and 15. The input match is better than 10 dB from 8-18 GHz and better than 8 dB from 6-8GHz. The output match is better than 10 dB from 6-18 GHz.

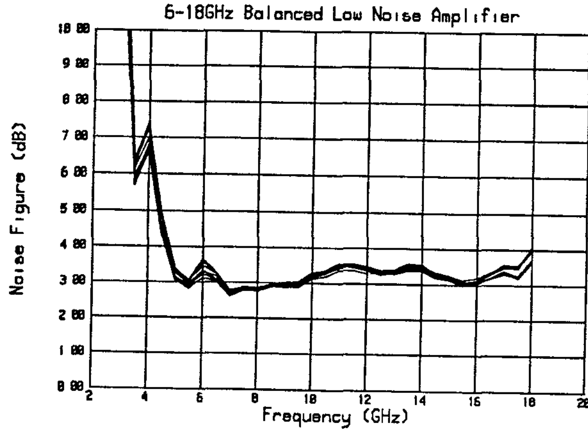

Figure 13. Balanced LNA Noise Figure

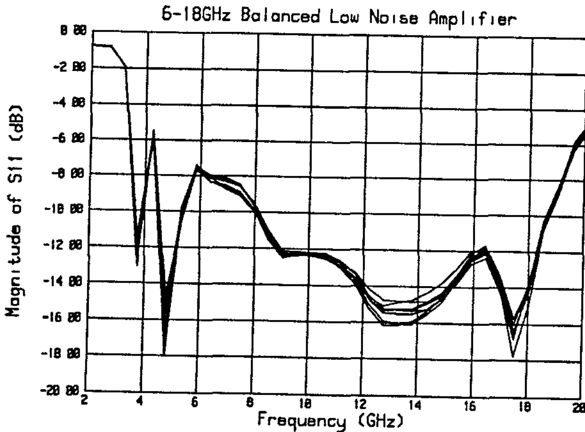

Figure 14. Balanced LNA Input Return Loss

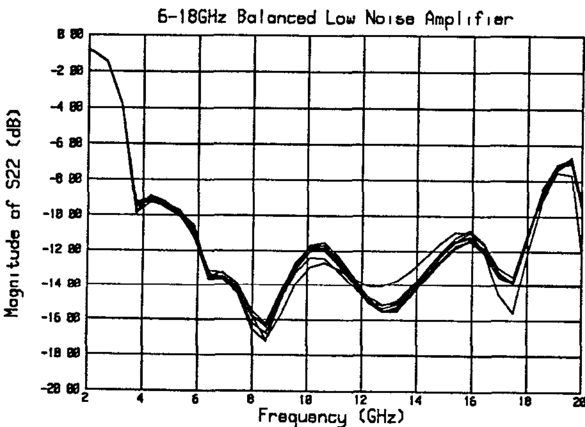

Figure 15. Balanced LNA Output Return Loss

MODELLING

The predicted data, using measured FET parameters of devices from the fabricated wafer, closely tracks the measured data. Noise parameters for the 0.25 micron FETs were obtained at the desired bias of 3v on the drain and a drain current of 50%Idss and 25%Idss, from an NP-5 (TM) measurement system. The amplifiers were simulated using these noise parameters and the nodal noise analysis of EESOF's Touchstone (TM) version 2.0. The use of nodal noise analysis allows the simulation to include the effects of feedback from the second stage to the first stage. This feedback is a result of biasing the two stage amplifiers in a parallel scheme to minimize chip bond pad requirements.

Specific areas of emphasis for passive modelling include: transmission lines (ZO,Keff,A), distributed resistors, distributed MIM capacitors. These techniques were developed in-house at Lockheed Sanders to design these amplifiers. The s-parameters for rectangular microstrip inductors were used in the 2-6 Ghz amplifiers. Lockheed Sanders maintains a library of these inductors.

CONCLUSION

This work has shown that low noise performance of ion-implant-process MMIC amplifiers can be achieved over broad bandwidths. An octave and a half bandwidth was shown at 2-6 Ghz and 6-18 GHz with less than 2.5 dB and 3 dB noise figure respectively. This process affords low risk, highly manufacturable MMICs for broadband low noise receiver applications.

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